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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/955,007	09/10/2001	Viktor Andrew Tymchenko	2207/353102	7863

7590 06/29/2004

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EXAMINER	
VOELTZ, EMANUEL T	

ART UNIT	PAPER NUMBER
2121	

DATE MAILED: 06/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/955,007	TYMCHENKO, VIKTOR ANDREW	
	Examiner	Art Unit	
	Emanuel T. Voeltz	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

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Examiner's Detailed Office Action

This action is in response to patent application number 09/955,007, filed January 22, 2002.

Claims 1-30 have been examined.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-13 and 15-30 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,713,030, granted to Evoy.

Regarding claim 1,

A computer system comprising: a processor having an input (see Evoy, figure 3, Processor Chip 102), and responsive to a signal at said input (see Evoy, figure 3, input to Processor Chip 114a), reducing a power consumption of said processor (see Evoy, figure 3, Clock Generator 114); and a power reduction circuit coupled to said input of said processor and providing a signal to said input of said processor in response to a failure condition affecting said processor such that the power consumption of said processor is periodically reduced (see Evoy, figure 3, Control Unit 110).

Regarding claim 2,

A computer system according to claim 1, wherein a first signal level of the signal at the input of the processor stops an internal clock of the processor.

Regarding claim 3,

A computer system according to claim 1, wherein said signal provided to said input of said processor in response to said failure condition comprises a periodic signal including at least a first signal level and a second signal level (see Evoy, figure 3, Clock Generator 114).

Regarding claim 4,

A computer system according to claim 1, further comprising a cooling fan directing air toward said processor, wherein said failure condition affecting said processor corresponds to a reduced performance of said cooling fan (see Evoy, figure 4, Fan 124).

Regarding claim 5,

A computer system according to claim 4, said power reduction circuit including a signal generator generating said periodic signal (see Evoy, figure 3, Control Unit 110 and Clock Generator 114).

Regarding claim 6,

A computer system according to claim 5, wherein said signal generator includes inputs corresponding to characteristics of said generated periodic signal (see Evoy, figure 3, Control Unit 110 and Clock Generator 114).

Regarding claim 7,

A computer system according to claim 5, wherein said signal generator includes an input corresponding to a duty cycle of said generated periodic signal and an input corresponding to a frequency or a period of said generated periodic signal (see Evoy, figure 3, Control Unit 110 and Clock Generator 114).

Regarding claim 8,

A computer system according to claim 1, wherein said power reduction circuit detects a temperature of said processor, wherein said failure condition affecting said processor is detected when said detected temperature of said processor is above a predetermined temperature (see Evoy, figure 3, Thermistor Circuit 116 and Comp. Circuit 118).

Regarding claim 9,

A computer system according to claim 1, wherein said power reduction circuit includes a sensor detecting a temperature of said processor, wherein said failure condition affecting said processor is detected when said sensed temperature of said processor is above a predetermined temperature (see Evoy, figure 3, Thermistor Circuit 116 and Comp. Circuit 118).

Regarding claim 10,

A computer system according to claim 9, wherein said sensor comprises a temperature sensor embedded in a heat sink attached to said processor (see Evoy, figure 4, Heat Sink 126).

Regarding claim 11,

A computer system according to claim 3, said power reduction circuit including a switch providing said periodic signal to said input in response to a presence of said

failure condition affecting said processor, said switch providing said second signal level to said input in response to an absence of said failure condition affecting said processor (see Evoy, figure 3, Control Unit 110 and Clock Generator 114).

Regarding claim 12,

A computer system according to claim 3, said power reduction circuit including a multiplexor providing said periodic signal to said input in response to a presence of said failure condition affecting said processor, said multiplexor providing said second signal level to said input in response to an absence of said failure condition affecting said processor (see Evoy, figure 3, Control Unit 110 and Clock Generator 114).

Regarding claim 13,

A computer system according to claim 1, wherein said failure condition affecting said processor is a thermal temperature condition corresponding to an overtemperature condition of said processor at or near said processor (see Evoy, figure 3, Thermistor Circuit 116 and Comp. Circuit 118).

Regarding claim 15,

An apparatus for reducing a power consumption of a processor, comprising: a signal generator generating a failure condition signal indicating a failure condition affecting said processor; and a power reduction circuit responsive to said failure condition signal and providing a periodic signal for periodically reducing a power consumption of said processor (see rejection to claim 1 above).

Regarding claim 16,

An apparatus according to claim 15, wherein said apparatus includes said processor, and said processor has a power consumption reduction input, wherein said

power reduction circuit provides said periodic signal to said power consumption reduction input of said processor in response to said failure condition signal (see rejection to claim 3 above).

Regarding claim 17

An apparatus according to claim 16, wherein an internal clock of the processor is stopped in response to the power consumption reduction input of the processor (see rejection to claim 2 above).

Regarding claim 18,

An apparatus according to claim 15, further comprising a cooling fan directing air toward said processor, wherein said failure condition affecting said processor corresponds to a reduced performance of said cooling fan (see rejection to claim 4 above).

Regarding claim 19,

An apparatus system according to claim 15, said power reduction circuit including a signal generator generating said periodic signal (see rejection to claim 5 above).

Regarding claim 20,

An apparatus according to claim 15, wherein said power reduction circuit includes a sensor detecting a temperature of said processor, wherein said failure condition affecting said processor is detected when said sensed temperature of said processor is above a predetermined temperature (see rejection to claim 8 above).

Regarding claim 21,

An apparatus according to claim 20, wherein said sensor comprises a temperature sensor embedded in a heat sink attached to said processor (see rejection to claim 10 above).

Regarding claim 22,

An apparatus according to claim 16, said power reduction circuit including a switch providing said periodic signal to said power condumption reduction input in response to a presence of said failure condition affecting said processor (see rejection to claim 11 above).

Regarding claim 23,

An apparatus according to claim 16, said power reduction circuit including a multiplexor providing said periodic signal to said power consumption reduction input in response to a presence of said failure condition affecting said processor (see rejection to claim 12 above).

Regarding claim 24,

An apparatus according to claim 15, wherein said failure condition affecting said processor is a thermal failure condition corresponding to an overtemperature condition of said processor at or near said processor (see rejection to claim 13 aboe).

Regarding claim 25,

A method of reducing a power consumption of a processor, comprising steps of: detecting a failure condition affecting said processor; and periodically reducing a power consumption of said processor in response to said step of detecting said failure condition (see rejection to claim 1 above).

Regarding claim 26,

A method according to claim 25, wherein said step of periodically reducing the power consumption of said processor comprises periodically stopping an internal clock of said processor (see rejection to claim 2 above).

Regarding claim 27,

A method according to claim 25, further comprising a step of measuring a temperature at or near said processor and providing said signal indicating a failure condition affecting said processor in response to said measured temperature (see rejection to claim 1 above).

Regarding claim 28,

A method according to claim 25, further comprising a step of providing said signal indicating a failure condition affecting said processor in response to a reduction in performance of a cooling fan (see rejection to claim 4 above).

Regarding claim 29,

A method according to claim 25, wherein said failure condition affecting said processor corresponds to an overtemperature condition of said processor at or near said processor (see rejection to claim 13 above).

Regarding claim 30,

A method according to claim 25, wherein said failure condition affecting said processor is a thermal failure condition affecting a temperature of said processor (see rejection to claim 1 above).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Evoy in view of U.S. Patent 6,141,762, granted to Nicol et al.

Regarding claim 14

A computer system according to claim 1, said computer system further comprising: at least one additional processor each having an input (see Nicol et al., figure 2, Processing Elements 101-104), wherein a power consumption of each processor is reduced in response to a first signal level of the input of that processor and is not reduced in response to a second signal level of the input of that processor (see Evoy, figure 3, input to Processor Chip 114a); and at least one additional power reduction circuit, each said additional power reduction circuit respectively corresponding to each said at least one additional processor and providing a signal to said input of said corresponding processor in response to a failure condition affecting the corresponding processor (see Nicol et al., figure 2, Processing Elements 101-104), wherein said signal provided to said input of said corresponding processor comprises a periodic signal including at least the first signal level and the second signal level (see Evoy, figure 3, Clock Generator 114).

The patent to Evoy sets forth a thermal management device and method for a single computer processor as seen from claims 1-13 above. Evoy, however, fails to disclose the use of redundant processors. The patent to Nicol et al. teaches the use of multi-processor elements in a power reduction system using redundant processors. It would have been obvious to one of ordinary skill in the art to use the thermal management system of Evoy using redundant processors as taught by Nicol et al. because thermal management of redundant processor systems would be just as necessary as they are for single processor systems. Many applications in the computing environment are turning to the use of redundant processors.

Prior Art of Record

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The various patents are cited for showing the general state of the art in thermal management of processors.

Correspondence Information

Any inquiries concerning this communication or earlier communications from the examiner should be directed to **Emanuel Todd Voeltz** who may be reached via telephone at

(703) 305-4563. The examiner can normally be reached Monday through Friday between the

hours of 8:00 a.m. and 5:00 p.m. eastern standard time.

If you need to send an Official facsimile transmission, please send it to **(703) 872-9306**. If you would like to send a Non-Official (draft) facsimile transmission the fax

is **(703) 746-5104**. If attempts to reach the examiner by telephone are unsuccessful, the Examiner's Supervisor, **Anthony Knight**, may be reached at **(703) 308-3179**.

Any response to this office action should be mailed too: **Director of Patents and Trademarks Washington, D.C. 20231**.

Moreover, hand-delivered responses should be delivered to the Receptionist, located on the **fourth floor of Crystal Park 11, 2121 Crystal Drive Arlington, Virginia**.

Emanuel Todd Voeltz
Primary Patent Examiner
Art Unit 2121
United States Department of Commerce
Patent & Trademark Office